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What is claimed is:

1. A deformable mirror system, comprising:

a deformable mirror being mechanically operated by at least one actuator, said at least one actuator having a signal electrode and a reference electrode, said at least one actuator converting an electrical signal into a mechanical motion, said at least one actuator receiving said electrical signal from an amplifier coupled to the signal electrode of said at least one actuator; and

electronics having at least one switch electrically coupled between said reference electrode and a reference node, said at least one switch having a closed state and an open state for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror.

2. The deformable mirror system according to Claim 1, wherein subsets of actuators are coupled to different amplifiers.

3. The deformable mirror system according to Claim 1, wherein said reference node is electrically coupled to analog ground.

1 4. The deformable mirror system according to Claim 1, wherein
2 the electronics further comprise addressing circuitry
3 electrically coupled to said at least one switch.

1 5. The deformable mirror system according to Claim 4, wherein
2 the addressing circuitry comprises circuitry to select zones
3 of switches.

1 6. The deformable mirror system according to Claim 1, wherein
2 the electronics further comprise at least one amplifier to
3 provide an electrical signal to the signal electrodes of a
4 subset of actuators.

1 7. The deformable mirror system according to Claim 1, wherein
2 the electronics further comprise at least one processor to
3 control the state of said at least one switch.

1 8. The deformable mirror system according to Claim 7, wherein
2 said processor receives data from an external system.

1 9. The deformable mirror system according to Claim 7, wherein
2 said electronics further comprise at least one amplifier,
3 said at least one processor providing command signals to
4 said at least one amplifier.

1 10. The deformable mirror system according to Claim 9, wherein
2 said at least one processor commands said at least one
3 amplifier to apply a desired surface figure to the mirror.

1 11. The deformable mirror system according to Claim 9, wherein
2 the electronics comprises at least two processors, at least
3 one processor providing command signals for said at least
4 one amplifier, at least one other processor selecting the
5 states of said at least one switch.

1 12. The deformable mirror system according to Claim 7, wherein
2 said at least one processor selects the states of switches
3 configured in zones of switches.

1 13. The deformable mirror system according to Claim 7, wherein
2 the electronics comprise a plurality of amplifiers, said at
3 least one processor commanding amplifiers providing
4 electrical signals to actuators configured in respective
5 zones of actuators.

1 14. The deformable mirror system according to Claim 7, wherein
2 said at least one processor executes at least one adaptive
3 optics computation.

1 15. The deformable mirror system according to Claim 1, wherein
2 the electronics comprise at least one current limiting
3 element.

1 16. The deformable mirror system according to Claim 1, wherein
2 said at least one switch is composed of at least one solid
3 state switch.

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1 17. The deformable mirror system according to Claim 1, wherein
2 said at least one switch is composed of two solid state
3 switches providing (i) a closed state having a low impedance
4 and (ii) an open state limiting forward and reverse leakage
5 current.

1 18. The deformable mirror system according to Claim 17, wherein
2 one of said two solid state switches is an N-Channel MOSFET
3 and the other of the two solid state switches is a P-Channel
4 MOSFET.

1 19. The deformable mirror system according to Claim 17, wherein
2 one of the two solid state switches is an N-channel FET
3 having a source (Sn), a drain (Dn), and a gate (Gn), and the
4 other of the two solid state switches is a P-channel FET
5 having a source (Sp), a drain (Dp), and a gate (Gp),
6 wherein:

7 (i) Dn is electrically coupled to said actuator
8 reference electrode;

9 (ii) Sn is electrically coupled to Dp;

10 (iii) Sp is electrically coupled to the reference node;

11 and

12 (iv) Gn and Gp are electrically coupled to circuitry to
13 apply at least one signal to selectably close and open said
14 at least one switch.

20. The deformable mirror system according to Claim 17, wherein
one of the two solid state switches is an N-channel FET
having a source (Sn), a drain (Dn), and a gate (Gn), and the
other of the two solid state switches is a P-channel FET
having a source (Sp), a drain (Dp), and a gate (Gp),
wherein:

7 (i) Dp is electrically coupled to said actuator
8 reference electrode;

9 (ii) Sp is electrically coupled to Dn;

10 (iii) Sn is electrically coupled to the reference node;

11 and

12 (iv) Gp and Gn are electrically coupled to circuitry to
13 apply at least one signal to selectably close and open said
14 at least one switch.

21. A deformable mirror system, comprising:

a deformable mirror being mechanically operated by at least one actuator, said at least one actuator having a signal electrode and a reference electrode, said at least one actuator converting an electrical signal into a mechanical motion, said at least one actuator receiving said electrical signal from a signal means coupled to said signal electrode of said at least one actuator; and

for said at least one actuator continuing to receive said electrical signal, means for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror.

1 22. An apparatus for controlling a deformable mirror
2 mechanically operated by at least one actuator, said at
3 least one actuator having a signal electrode and a reference
4 electrode, the apparatus comprising:

5 electronics coupled to said at least one actuator, said
6 electronics having at least one switch electrically coupled
7 between said reference electrode of said at least one
8 actuator and a reference node, said at least one switch
9 having a closed state and an open state for selectably
10 enabling and disabling said at least one actuator to control
11 the mechanical operation of the mirror.

1 23. The apparatus according to Claim 22, wherein subsets of
2 actuators are coupled to different amplifiers.

1 24. The apparatus according to Claim 22, wherein said reference
2 node is electrically coupled to analog ground.

1 25. The apparatus according to Claim 22, further comprising
2 addressing circuitry to select said at least one switch.

1 26. The apparatus according to Claim 25, wherein the addressing
2 circuitry comprises circuitry to select zones of switches.

1 27. The apparatus according to Claim 22, wherein the electronics
2 further comprise at least one amplifier to provide
3 electrical signals to the signal electrodes of a subset of
4 actuators.

1 28. The apparatus according to Claim 22, wherein the electronics
2 further comprise at least one processor to control the state
3 of said at least one switch.

1 29. The apparatus according to Claim 28, wherein the processor
2 receives data from an external system.

1 30. The apparatus according to Claim 28, wherein the electronics
2 further comprise at least one amplifier, said at least one
3 processor providing command signals to said at least one
4 amplifier.

1 31. The apparatus according to Claim 30, wherein said at least
2 one processor commands said at least one amplifier to apply
3 a desired surface figure to the mirror.

1 32. The apparatus according to Claim 30, wherein the electronics
2 comprise at least two processors, at least one processor
3 providing command signals for said at least one amplifier,

4 at least one other processor selecting the states of said at
5 least one switch.

1 33. The apparatus according to Claim 28, wherein said at least
2 one processor selects the states of switches configured in
3 zones of switches.

Al 1 34. The apparatus according to Claim 28, wherein the electronics
2 comprise a plurality of amplifiers, said at least one
3 processor commanding said amplifiers providing electrical
4 signals to said actuators configured in zones of actuators.

1 35. The apparatus according to Claim 28, wherein said at least
2 one processor executes at least one adaptive optics
3 computation.

1 36. The apparatus according to Claim 22, wherein the electronics
2 comprises at least one current limiting element.

1 37. The apparatus according to Claim 22, wherein said at least
2 one switch is composed of at least one solid state switch.

1 38. The apparatus according to Claim 22, wherein said at least
2 one switch is composed of two solid state switches providing

3 (i) a closed state having a low impedance and (ii) an open
4 state limiting forward and reverse leakage current.

1 39. The apparatus according to Claim 38, wherein one of the two
2 solid state switches is an N-Channel MOSFET and the other of
3 the two solid state switches is a P-Channel MOSFET.

1 40. The apparatus according to Claim 38, wherein one of the two
2 solid state switches is an N-channel FET having a source
3 (Sn), a drain (Dn), and a gate (Gn), and the other of the
4 two solid state switches is a P-channel FET having a source
5 (Sp), a drain (Dp), and a gate (Gp), wherein:

6 (i) Dn is electrically coupled to the actuator
7 reference electrode;

8 (ii) Sn is electrically coupled to Dp;

9 (iii) Sp is electrically coupled to the reference node;

10 and

11 (iv) Gn and Gp are electrically coupled to circuitry to
12 apply at least one signal to selectably close and open said
13 at least one switch.

1 41. The apparatus according to Claim 38, wherein one of the two
2 solid state switches is an N-channel FET having a source
3 (Sn), a drain (Dn), and a gate (Gn), and the other of the

4 two solid state switches is a P-channel FET having a source
5 (Sp), a drain (Dp), and a gate (Gp), wherein:

6 (i) Dp is electrically coupled to the actuator
7 reference electrode;

8 (ii) Sp is electrically coupled to Dn;

9 (iii) Sn is electrically coupled to the reference node;

10 and

11 (iv) Gp and Gn are electrically coupled to circuitry to
12 apply at least one signal to selectably close and open said
13 at least one switch.

42. An apparatus for controlling a deformable mirror mechanically operated by at least one actuator, said at least one actuator comprising a signal electrode and a reference electrode, said at least one actuator receiving an electrical signal at the signal electrode, the apparatus comprising:

for said at least one actuator continuing to receive said electrical signal, means for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror.

1 43. An apparatus for controlling a deformable mirror
2 mechanically operated by at least one actuator, said at
3 least one actuator comprising a signal electrode and a
4 reference electrode, said at least one actuator receiving an
5 electrical signal at the signal electrode, the apparatus
6 comprising:

7 electronics coupled to said at least one actuator, the
8 electronics comprising (i) an amplifier having an output
9 coupled to the signal electrodes of said at least one
10 actuator, and (ii) at least one switch electrically coupled
11 between the reference electrode of said at least one
12 actuator and a reference node providing a signal reference,
13 said at least one switch having a closed state and an open
14 state for selectably enabling and disabling said at least
15 one actuator to control the mechanical operation of the
16 mirror;

17 addressing circuitry to enable at least one switch
18 coupled to the addressing circuitry, the addressing
19 circuitry converting an address signal to a switch
20 selection; and

21 at least one processor executing processor
22 instructions, the processor instructions comprising
23 instructions to:

24 issue address signals to the addressing circuitry;

25 and

26 in coordination with issuing the address signals,
27 direct corresponding actuator commands to the amplifier
28 to supply the electrical signal to the signal electrode
29 of said at least one actuator to mechanically operate
30 the deformable mirror.

1 44. The apparatus according to Claim 43, wherein, to coordinate
2 issuing address signals and directing actuator commands, the
3 processor instructions further comprise instructions to:

4 for a given actuator, direct the amplifier to output a
5 first signal, the first signal corresponding to a signal
6 most recently applied to the given actuator;

7 issue a first address signal to close a switch
8 corresponding to the given actuator;

9 direct the amplifier to output a second signal
10 corresponding to the signal determined by the processor to
11 be directed to the given actuator; and

12 issue a second address signal to open the switch
13 corresponding to the given actuator.

1 45. The apparatus according to Claim 43, wherein the
2 instructions further comprise instructions to parse a
3 command frame, the command frame including actuator
4 commands.

1 46. The apparatus according to Claim 45, wherein the command
2 frame is received from an external system.

1 47. The apparatus according to Claim 45, wherein the
2 instructions further comprise instructions to process the
3 actuator commands in the command frame to limit inter-
4 actuator stroke applied to the mirror.

1 48. The apparatus according to Claim 43, wherein the
2 instructions to direct actuator commands to the amplifier
3 comprise instructions to limit current flow through the
4 switches.

1 49. The apparatus according to Claim 43, wherein the
2 instructions to issue address signals to the addressing
3 circuitry comprise instructions to issue address signals to
4 the addressing circuitry for zones of actuators.

1 50. The apparatus according to Claim 43, wherein the
2 instructions further comprise instructions to conserve power
3 consumed by the apparatus.

1 51. The apparatus according to Claim 50, wherein the
2 instructions to conserve power consumed by the apparatus

further comprise instructions to retain a figure on the mirror while conserving power consumed by the apparatus.

52. The apparatus according to Claim 43, wherein the processor includes a plurality of processors.

1 53. A method for controlling a deformable mirror mechanically
2 operated by actuators in an actuator array, the method
3 comprising:

4 selectably applying a reference signal to a first
5 electrode of at least one actuator; and

6 providing a command signal to a second electrode of
7 said at least one actuator to operate the mirror.

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1 54. The method according to Claim 53, further comprising driving
2 an initial command signal to the second electrode of said at
3 least one actuator prior to applying the reference signal to
4 the first electrode.

1 55. The method according to Claim 53, further comprising parsing
2 a command frame, the command frame including actuator
3 commands.

1 56. The method according to Claim 55, wherein the command frames
2 are received from an external system.

1 57. The method according to Claim 55, further comprising
2 processing the actuator commands in the command frame to
3 limit inter-actuator stroke applied to the mirror.

1 58. The method according to Claim 53, wherein driving a command
2 signal to said at least one actuator comprises limiting
3 current flow through the switches.

1 59. The method according to Claim 53, further comprising
2 applying a reference signal to first electrodes of actuators
3 configured in a zone of actuators.

1 60. The method according to Claim 53, further comprising
2 conserving power consumed.

1 61. The method according to Claim 60, wherein conserving power
2 consumed by the apparatus comprises retaining a figure on
3 the mirror while conserving power.

means for driving a command signal to the first electrodes of said actuators; and

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